

<b>Notice of Allowability</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/711,543	HUANG ET AL.	
	Examiner Vincent E. Kovalick	Art Unit 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1.  This communication is responsive to Applicant's Amendment dated October 11, 2007.
2.  The allowed claim(s) is/are 1-14.
3.  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a)  All
  - b)  Some\*
  - c)  None
 of the:
  1.  Certified copies of the priority documents have been received.
  2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3.  Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.  
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4.  A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5.  CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
  - (a)  including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
    - 1)  hereto or 2)  to Paper No./Mail Date \_\_\_\_\_.
  - (b)  including changes required by the attached Examiner's Amendment / Comment or in the Office action of
 Paper No./Mail Date \_\_\_\_\_.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6.  DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

#### Attachment(s)

1.  Notice of References Cited (PTO-892)
2.  Notice of Draftsperson's Patent Drawing Review (PTO-948)
3.  Information Disclosure Statements (PTO/SB/08),  
Paper No./Mail Date 7/16/07
4.  Examiner's Comment Regarding Requirement for Deposit  
of Biological Material
5.  Notice of Informal Patent Application
6.  Interview Summary (PTO-413),  
Paper No./Mail Date \_\_\_\_\_.
7.  Examiner's Amendment/Comment
8.  Examiner's Statement of Reasons for Allowance
9.  Other \_\_\_\_\_.

## DETAILED ACTION

### *Response to Amendment*

1. This Office Action is in response to Applicant's Amendment and Response to Office Action dated October 11, 2007, in response to USPTO Office Action dated July 12, 2007.

Applicant's remarks and arguments relative to claim 4 have merit and are sufficient to place the application in a condition for allowance as set forth hereinbelow.

### *Allowable Subject Matter*

2. Claims 1-14 are allowed.

3. The following is an examiner's statement of reasons for allowance:

Regarding claim 1, the major difference between the teachings of the prior art of record (Deane et al., Pub. No. 2006/0097965; Sakashita et al., Pub No. 2004/0169665 and Iwasaki, Pub. No. 2004/017931) and that of the instant invention is that said prior art of record **does not teach** a control circuit, for an LCD device having a power module, a host control unit, and an image display unit, the power module supplying a plurality of potential levels for the LCD device, the control unit controlling a plurality of gate driving signals and a plurality of source driving signals for the image display unit, the control circuit comprising: a signal delay unit, coupled to the image display unit; and a signal detecting unit, coupled to the host control unit, wherein the signal detecting unit detects an on/off status of the LCD device from the host control unit, provides a disable signal to the power module, such that the voltage potential levels are disabled except a pixel transistor turning-on level, a plurality of pixel transistors of the image display unit are discharged via sources of the pixel transistors, and provides an all-gate-on signal to the signal delay unit, the all-gate-on signal is delayed for a first delay time by the signal delay unit and outputs to the image display unit.

Relative to claim 4, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** a method of discharging pixel transistors of an LCD device, comprising: detecting whether the LCD device stops displaying an image; providing a first signal to disable a power module of the LCD device and turn off a pixel transistor turn-on potential level after a first delay time; and providing a second signal to turn on all the pixel transistors after a second delay time.

Regarding claim 7, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** an Applied Specific Integrated Circuit (ASIC), for a capacitor charging/discharging device, having a plurality of capacitors, comprising: a host control unit; a signal detecting unit, receiving a first disable signal outputted from the host control unit and outputting a second disable signal to a power supply module outside of the ASIC, for disabling a part of the power supply module simultaneously, and disabling other part of the power supply module which controls the capacitors after a first delay time; and a delay unit, receiving a second signal from the signal detecting unit, and outputting to the capacitor charging/discharging device after having paused for a second delay time, such that a plurality of switches controlling the capacitors are turned on.

Relative to claim 8, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** an LCD panel system, for operating an LCD panel controlled by at least a plurality of source driving signals and a plurality of gate driving signals, comprising: a control circuit, outputting a plurality of data and a plurality of control signals; a pixel array, coupled to the control circuit, having a plurality of pixels arranged in an array, wherein each of the pixels corresponds to a transistor for receiving at least one of the data provided from the control circuit and at least one of the control signals for displaying an image; a power module, for supplying a plurality of potential levels to the LCD panel and receiving at least a part of the control signals from the control circuit, wherein when the control circuit detects the LCD panel has stopped to display the image, a first signal and a second signal are transmitted, wherein the first signal disables the power module and turns off a pixel transistor turn-on level after a first delay time, and the second signal turns on gates of the transistors corresponding to all of the pixels after a second delay time.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Response to Applicant's Remarks***

4. The allowance of this case renders moot Applicant's arguments relative to claim 4.

***Conclusion***

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Pub. No.	US 2004/0147113	Yamazaki et al.
Pub. No.	US 2003/0234780	Hsieh et al.
Pub. No.	US 2003/0146907	Boals et al.
Pub. No.	US 2002/0158587	Komiya

***To Respond***

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent E. Kovalick whose telephone number is 571-272-7669. The examiner can normally be reached on Monday-Thursday 7:30- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Vincent E. Kovalick  
November 8, 2007



BIPIN SHALWALA  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600